



RAJEEV KUMAR RANJAN

Associate Professor

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Research Interests

VLSI and integrated circuit design with focus on analog and mixed-signal VLSI, low-power CMOS circuits, and advanced digital IC design. Neuromorphic and in-memory computing hardware, crossbar and memristor-enabled architectures, and AI/edge hardware accelerators for energy-efficient intelligent systems. ASIC design for strategic applications including space electronics, radiation and X-ray instrumentation, and ED-XRF-based sensing platforms.

Teaching Interests

Digital VLSI Circuits and Systems, Computer Aided Designs for Neuromorphic Computing.
Analog and mixed VLSI design: Analog Filter, Oscillator, PID Controllers, Driver System for Satellite Torquer System.
CMOS based digital design and different types of challenges. TSMC 180 nm PDK, 180 nm SCL PDK, UMC 180 nm, 65 nm, 28 nm etc.

Employment History

Employer	Post	Period of Employment	
		From	To
Indian Institute of Technology, ISM Dhanbad	Associate Professor	22.03.2023	Continuing
Indian Institute of Technology, ISM Dhanbad	Assistant Professor	30.11.2010	21.03.2023
Sant Longowal Institute of Engineering and Technology, Longowal, Punjab, India (MHRD Funded Deemed University)	Assistant Professor	Aug, 2007	Nov, 2010
North Eastern Regional Institute of Technology, Itanagar, Arunachal Pradesh, India (MHRD Funded Deemed University)	Assistant Professor	Apr, 2007	Jul, 2007
Central Electronics Engineering Research Institute, Pilani, Rajasthan, India	Project Scientist	Jul, 2004	Aug, 2005

Academic Qualifications

- B. Tech., Electronics & Communication Engineering (2000 – 2003)
- M. Tech., Electronics Design and Technology (2005 – 2007)
- Ph.D., Microelectronics and VLSI Design (Oct. 2011 – Nov. 2016)

Sponsored Projects Handled

Sl. No.	Title of Project	Role	Funding Agency & Project No.	Grant (Rs.)	Duration	Status
1	Ultra-Low Power Neuro-morphic Spiking Architecture for Assistive Smart Glasses	PI	MEITY, New Delhi (MietY/2023-2024/1012/ECE)	112 L	01-07-2023 (60 Months)	Ongoing
2	Memristor based Multilayer Neural Networks (MNN) and its Application in Neuromorphic System	PI	CSIR(40)/2023-2024/1045/ECE	38 L	01-09-2023 (36 Months)	Ongoing
3	Design and Implementation of a Light-to-digital Converter for Photoplethysmogram (PPG) Sensor Application	Team Member	CSIR-CEERI	17 L	16-06-2021 (36 Months)	Completed
4	Memristor Based Biosensor Design for COVID-19	PI	MHRD (SICRG/2020-2021/740/ECE)	10 L	09-11-2020 (37 Months)	Completed
5	Auto irrigation and Soil Monitoring System for COVID-19 Migrants Engagement	PI	IEEE (2020-2021/718/ECE)	7 L	23-06-2020 (24 Months)	Completed
6	FIST-2019 Project of Department of Electronics Engineering	Member (VLSI Implementation)	DST, Govt. of India (TPN-31665)	190 L	07-01-2020 (60 Months)	Completed
7	Determination of 120W Street Light Parameters	PI	Dhanbad Municipal Corporation (TEST/5013/2018-2019)	84,746	2018-2019	Completed
8	Determination of 90W Street Light Parameters	PI	Dhanbad Municipal Corporation (TEST/5014/2018-2019)	59,322	2018-2019	Completed
9	Quotation for Testing of LED Street Light	PI	Office of Dy. Commissioner of Customs, Banskop (CONS/3508/2017-2018)	17,400	2017-2018	Completed
10	Design of New Low Power, Low Voltage and High Bandwidth Current Mode Building Block (CMBB)	PI	Minor Research Project, TEQIP-II	2 L	20-01-2017	Completed

Outreach Programme

S. No.	Title of Course	Role	Authority	Grant (Rs.)	Year
1	Advanced Analog Signal Processing and Generating Circuits	Co-Consultant	Dept. of ECE, IIT(ISM) Dhanbad	0.48 L	2014
2	Current Mode Analog Circuits	Co-Consultant	Dept. of ECE, IIT(ISM) Dhanbad	0.70 L	2013
3	Advanced Analog Circuits using Current Mode Building Blocks	Co-Consultant	Dept. of ECE, IIT(ISM) Dhanbad	1 L	2015
4	DST (SERB) KARYASHALA	Co-Coordinator	Dept. of ECE, IIT(ISM) Dhanbad	5 L	2022
5	AICTE Margdarshan Scheme Training Program	Coordinator	Dept. of ECE, IIT(ISM) Dhanbad	18 L	2024
6	GIAN Course on (virtual mode) “Memristor and its application in Neuromorphic computations”	Coordinator	Ministry of Education, India	2.90 L	2025
7	IEP Course on “Advanced Semiconductor Design Techniques Using Modern VLSI EDA Tools”	Coordinator	Ministry of Electronics and Information Technology, India	5 L	July 2026
8	Refresher Course on “Device-Circuit Co-Design: From Emerging Materials to Intelligent Systems”	Co-Coordinator	Malaviya Mission Teacher Training Centre, IIT (ISM) Dhanbad	12 Lakhs	Aug. 2026

International Journal Publications

Year 2026

- [1] S. Bediga, T. K. Sharma, A. Kalakola, V. Upadhyay, **R. K. Ranjan**, and S.-M. Kang, “Compact Memristor Emulator with SDDP for Integrated Neuromorphic Temporal Learning,” **IEEE Transactions on Circuits and Systems for Artificial Intelligence**, Mar. 2026.
DOI:[10.1109/TCASAI.2026.3676004](https://doi.org/10.1109/TCASAI.2026.3676004).
- [2] V. Upadhyay, N. Singhal, B. S. Makhdoomi, V. Saxena, **R. K. Ranjan**, and S.-M. Kang, “Design of a 65 nm CMOS Neuromorphic Circuit for Sequential Alphanumeric Pattern Detection with Experimental Verification,” **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, Mar. 2026.
DOI:[10.1109/TVLSI.2026.3674147](https://doi.org/10.1109/TVLSI.2026.3674147).
- [3] R. Jaiswal, B. S. Makhdoomi, V. Upadhyay, and **R. K. Ranjan**, “An event-driven bioinspired associative learning circuit using CCTA-controlled memcapacitive emulator with spike generation”, **Integration**, p. 102717, Mar. 2026.
DOI:[10.1016/j.vlsi.2026.102717](https://doi.org/10.1016/j.vlsi.2026.102717).
- [4] A. Kalakola, B. S. Makhdoomi, R. Ranjan, **R. K. Ranjan**, and S. Minaei, “A compact memristor emulator for energy efficient neuron application,” **AEU - International Journal of Electronics and Communications**, vol. 208, p. 156260, Feb. 2026.
DOI:[10.1016/j.aeue.2026.156260](https://doi.org/10.1016/j.aeue.2026.156260).

- [5] V. Upadhyay, K. K. Kumar, R. K. Gupta, V. Saxena, and **R. K. Ranjan**, "A Passive Symmetrical Memristor Emulator Circuit with Applications in Square Wave Generator, Chaotic Oscillator, and Digital Logic Gates," **Circuits, Systems, and Signal Processing**, Feb. 2026.
DOI:[10.1007/s00034-025-03479-x](https://doi.org/10.1007/s00034-025-03479-x).

Year 2025

- [6] N. Kumar and **R. K. Ranjan**, "Morphological tuning of VO₂ nanowires to develop VO₂/CuWO₄ nanocomposite for improved supercapacitance as a binder-free electrode," in **Inorganic Chemistry Communications**, 2025.
DOI:[10.1016/j.inoche.2025.115668](https://doi.org/10.1016/j.inoche.2025.115668).
- [7] P. Kumar, **R. K. Ranjan** and S. -M. Kang, "An Ultra-Low Power 1.2 pJ/Spike Fully CMOS Spiking Neuron and Its Application," in **IEEE Transactions on Nanotechnology**, vol. 24, pp. 462-468, 2025.
DOI:[10.1109/TNANO.2025.3613362](https://doi.org/10.1109/TNANO.2025.3613362).
- [8] Verma, J.S., Kumar, P., Makhdoomi, B.S., **Ranjan, R.K.** and Kang, S.M., 2025. "Memristor-Emulator-Based Crossbar Array for Object Detection and Recognition". **IEEE Transactions on Circuits and Systems I: Regular Papers**.
DOI:[10.1109/TCSI.2025.3553058](https://doi.org/10.1109/TCSI.2025.3553058).
- [9] Kumar, N., Sankaranarayanan, S., Kandasamy, M., Husain, A. and **Ranjan, R.K.**, 2025. Performance of Tri-metallic Zn-ion battery cathode using hybrid morphology of VO₂/CuWO₄ nanocomposite. **Cryst Eng Comm**.
DOI:[10.1039/D5CE00529A](https://doi.org/10.1039/D5CE00529A).
- [10] Kumar, P., Makhdoomi, B.S., Verma, J.S., Sonwani, S., Ranjan, R., and **Ranjan, R.K.**, 2025. Experimental validation of a high-frequency memristor emulator based on CCCCTA framework and its application in chaos circuit. **AEU - International Journal of Electronics and Communications**, 190, 155624.
DOI:[10.1016/j.aeue.2024.155624](https://doi.org/10.1016/j.aeue.2024.155624).

Year 2024

- [11] P. Kumar, **R. K. Ranjan** and S. -M. Kang, "Memristor-Emulating-Integrate-and-Fire Neuron-Based Fully Neuromorphic Framework for Pattern Recognition," in **IEEE Transactions on Circuits and Systems II: Express Briefs**, vol. 71, no. 12, pp. 5024-5028, Dec. 2024.
DOI :[10.1109/TCSII.2024.3439687](https://doi.org/10.1109/TCSII.2024.3439687).
- [12] Kumar, P., Bhat, A.M., Sharma, P.K. and **Ranjan, R.K.**, 2024. A novel and compact MOSFET-C only based grounded meminductor emulator and its application. **AEU - International Journal of Electronics and Communications**, 183, p.155378.
DOI :[10.1016/j.aeue.2024.155378](https://doi.org/10.1016/j.aeue.2024.155378).
- [13] Kumar, P., **Ranjan, R.K.** and Kang, S.M., 2024. A Memristor Emulation in 180-nm CMOS Process for Spiking Signal Generation and Chaos Application. **IEEE Transactions on Circuits and Systems I: Regular Papers**, 71(4), pp.1757-1770.
DOI :[10.1109/TCSI.2023.3348695](https://doi.org/10.1109/TCSI.2023.3348695).
- [14] N. Raj, S. Dutta, **R. K. Ranjan**, P. K. Das, D. K. Singh, and Hakan Kuntman, "VDTA based transadmittance mode instrumentation amplifier with experimental results," *International Journal of Electronics*, vol. 112, no. 10, pp. 2194-2211, Dec. 2024.
DOI :[10.1080/00207217.2024.2439182](https://doi.org/10.1080/00207217.2024.2439182).
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DOI :[10.1016/j.aeue.2024.155215](https://doi.org/10.1016/j.aeue.2024.155215).

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DOI: [10.1109/MCAS.2024.3353151](https://doi.org/10.1109/MCAS.2024.3353151).
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DOI : [10.1016/j.chaos.2024.114824](https://doi.org/10.1016/j.chaos.2024.114824).
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DOI: [10.1109/ACCESS.2023.3344311](https://doi.org/10.1109/ACCESS.2023.3344311).
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DOI: [10.1080/00207217.2023.2267218](https://doi.org/10.1080/00207217.2023.2267218).
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- [23] F. Khateb, M. Kumngern, T. Kulej, and **R. K. Ranjan**, “0.5 V Multiple-Input Multiple-Output Differential Difference Transconductance Amplifier and Its Applications to Shadow Filter and Oscillator,” **IEEE Access**, vol. 11, pp. 31212–31227, 2023.
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DOI : [10.1007/s13369-022-07559-x](https://doi.org/10.1007/s13369-022-07559-x).
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DOI : [10.1016/j.aeue.2022.154500](https://doi.org/10.1016/j.aeue.2022.154500).
Year 2022
- [30] Prasad, S.S., Kumar, P., Raj, N., Sharma, P.K., Priyadarshini, B., **Ranjan, R.K.** and Prommee, P., 2022. A compact floating and grounded memristor model using single active element. **AEU - International Journal of Electronics and Communications**, 157, p.154426.
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DOI : [10.1109/ICJECE.2022.3182711](https://doi.org/10.1109/ICJECE.2022.3182711).
- [32] Raj, N., **Ranjan, R.K.** and James, A., 2022. Chua's Oscillator With OTA Based Memcapacitor Emulator. **IEEE Transactions on Nanotechnology**, 21, pp.213-218.
DOI : [10.1109/TNANO.2022.3168154](https://doi.org/10.1109/TNANO.2022.3168154).
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DOI : [10.1007/s13369-021-06488-5](https://doi.org/10.1007/s13369-021-06488-5).
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- [34] Tasneem, S., **Ranjan, R.K.** and Paul, S.K., 2021. Performance Enhancement of Current Follower Transconductance Amplifier (CFTA) and its Application as Filter. **Journal of Circuits, Systems, and Computers**.
DOI : [10.1142/S0218126622500244](https://doi.org/10.1142/S0218126622500244).
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DOI : [10.1109/ACCESS.2021.3081581](https://doi.org/10.1109/ACCESS.2021.3081581).
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DOI : [10.1109/ACCESS.2021.3078189](https://doi.org/10.1109/ACCESS.2021.3078189).
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DOI : [10.3390/electronics10080911](https://doi.org/10.3390/electronics10080911).
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- [58] Mazumdar, K., **Ranjan, R.K.**, Shankar, R., Priyadarshini, B. and Ghosal, A., 2017. Modern comparative approach for carrier transport in InAlN/AlN superlattice device with characteristics and modelling using nitride (¹⁴N, ¹⁵N) isotopes. **Superlattices and Microstructures**, 103, pp.190-194. DOI : [10.1016/j.spmi.2017.01.008](https://doi.org/10.1016/j.spmi.2017.01.008).
- [59] **Ranjan, R.K.**, Rani, N., Pal, R., Paul, S.K. and Kanyal, G., 2017. Single CCTA based high frequency floating and grounded type of incremental/decremental memristor emulator and its application. **Microelectronics Journal**, 60, pp.119-128. DOI : [10.1016/j.mejo.2016.12.004](https://doi.org/10.1016/j.mejo.2016.12.004).

Year 2016

- [60] **Ranjan, R.K.**, Choubey, C.K., Nagar, B.C. and Paul, S.K., 2016. Comb filter for elimination of unwanted power line interference in biomedical signal. **Journal of Circuits, Systems and Computers**, 25(06), p.1650052. DOI : [10.1142/S0218126616500523](https://doi.org/10.1142/S0218126616500523).
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- [62] **Ranjan, R. K.**, Kumar, K., Rani, N., Paul, S.K. and Akashe, S., 2016. A powerline filter circuit design for biomedical applications. **Journal of Computational and Theoretical Nanoscience**, 13(5), pp.3345-3351. DOI : [10.1166/jctn.2016.4997](https://doi.org/10.1166/jctn.2016.4997).

Year 2014

- [63] **Ranjan, R.K.**, Yalla, S.P., Sorya, S. and Paul, S.K., 2014. Active comb filter using operational transconductance amplifier. **Active and Passive Electronic Components**, 2014(1), p.587932. DOI : [10.1155/2014/587932](https://doi.org/10.1155/2014/587932).

Year 2013

- [64] Ghosh, M., Paul, S.K., **Ranjan, R.K.** and Ranjan, A., 2013. Third order universal filter using single operational transresistance amplifier. **Journal of Engineering**, 2013(1), p.317296. DOI : [10.1155/2013/317296](https://doi.org/10.1155/2013/317296).

International/National Conferences Publications

Year 2025

- [1] P. Srivastava, P. Kumar and **R. K. Ranjan**, "2-MOSFET Dynamic Threshold-Based Reversible & Bipolar Unbiased Inverse-Memristor Emulator," *2025 14th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, Dresden, Germany, 2025, pp. 1-5.// DOI: [10.1109/MOCAST65744.2025.11083917](https://doi.org/10.1109/MOCAST65744.2025.11083917).
- [2] P. K. Sharma and **R. K. Ranjan**, "Mem-Element Emulators: An Opportunity for Next Generation Human Centered Computing," in **Intelligent Human Centered Computing**, S. Bhattacharyya, J. S. Banerjee, D. De, and M. Mahmud, Eds. Springer Tracts in Human-Centered Computing, Springer, Singapore, 2025. DOI:[10.1007/978-981-96-1761-6_9](https://doi.org/10.1007/978-981-96-1761-6_9).

Year 2024

- [3] Makhdoomi, B.S. and **Ranjan, R.K.**, 2024. Memristor Emulator Circuit Design using MOCCII. In *2024 International Conference on Modeling, Simulation & Intelligent Computing (MoSICom)*, Dubai, United Arab Emirates (pp. 17-22). IEEE. DOI: [10.1109/MoSICom63082.2024.10881881](https://doi.org/10.1109/MoSICom63082.2024.10881881).
- [4] N. Raj, P. Deepthi, K. J. Dayanand and **R. K. Ranjan**, "Generic Memcapacitor Design with Tunable and Resistorless Features and Experimental Investigations," *2024 International Conference on Modeling, Simulation & Intelligent Computing (MoSICom)*, Dubai, United Arab Emirates, 2024, pp. 369-372, DOI: [10.1109/MoSICom63082.2024.10881752](https://doi.org/10.1109/MoSICom63082.2024.10881752).
- [5] P. K. Sharma and **R. K. Ranjan**, "A Dual-Mode High-Frequency Grounded Memristor Emulator Circuit," in **Emerging VLSI Devices, Circuits and Architectures**, A. Gupta, J. G. Pandey, N. Chaturvedi, and D. Dwivedi, Eds. Lecture Notes in Electrical Engineering, vol. 1234, Springer, Singapore, 2025. DOI:[10.1007/978-981-97-5269-0_10](https://doi.org/10.1007/978-981-97-5269-0_10).
- [6] P. K. Sharma, A. Mohanty, P. Kumar, **R. K. Ranjan** and R. Kumar, "Investigation of Aluminum With Group III Compounded Semiconductor Material in JLTFT," *2024 IEEE International Conference on Smart Power Control and Renewable Energy (ICSPCRE)*, Rourkela, India, 2024, pp. 1-4, DOI: [10.1109/ICSPCRE62303.2024.10674867](https://doi.org/10.1109/ICSPCRE62303.2024.10674867).
- [7] S. Tasneem, **R. K. Ranjan**, and S. K. Paul, "Electronically Tunable Fractional-Order Universal Filter," in **VLSI for Embedded Intelligence**, A. Gupta, J. G. Pandey, N. Chaturvedi, and D. Dwivedi, Eds. Lecture Notes in Electrical Engineering, vol. 1210, Springer, Singapore, 2025. DOI:[10.1007/978-981-97-3756-7_2](https://doi.org/10.1007/978-981-97-3756-7_2).

Year 2023

- [8] Dutta, S., **Ranjan, R.K.** and Singh, D.K., 2023, April. Designing Tuneable Circuits Using the DDCC2TA for Square, Triangular Wave Generation and Pulse Width Modulation. In *2023 Second International Conference on Electrical, Electronics, Information and Communication Technologies (ICEEICT)* (pp. 1-5). IEEE.
DOI: [10.1109/ICEEICT56924.2023.10157604](https://doi.org/10.1109/ICEEICT56924.2023.10157604).

Year 2022

- [9] Sharma, P.K., Kumar, P. and **Ranjan, R.K.**, 2022, October. A high-frequency flux controlled grounded memristor emulator. In *14th International Conference on Information Technology and Electrical Engineering (ICITEE)* (pp. 64-67). IEEE.
DOI: [10.1109/ICITEE56407.2022.9954099](https://doi.org/10.1109/ICITEE56407.2022.9954099).
- [10] Sharma, P.K., Prasad, S.S., Tasneem, S. and **Ranjan, R.K.**, 2022, May. A new Grounded Memristor Emulator using DVCC and OTA. In *19th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON)* (pp. 1-4). IEEE.
DOI: [10.1109/ECTI-CON54298.2022.9795412](https://doi.org/10.1109/ECTI-CON54298.2022.9795412).
- [11] Prasad, S.S., Raj, N., Sharma, P.K. and **Ranjan, R.K.**, 2022, May. Grounded memristor emulator using single active block. In *19th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON)* (pp. 1-4). IEEE.
DOI: [10.1109/ECTI-CON54298.2022.9795587](https://doi.org/10.1109/ECTI-CON54298.2022.9795587).

Year 2021

- [12] Prasad, S.S., Tasneem, S., Priyadarshini, B. and **Ranjan, R.K.**, 2021, September. Electronic Tunable Bi-Quad Filter Using MO-CCCDTA. In *Fourth International Conference on Electrical, Computer and Communication Technologies (ICECCT)* (pp. 1-6). IEEE.
DOI: [10.1109/ICECCT52121.2021.9616870](https://doi.org/10.1109/ICECCT52121.2021.9616870).

Year 2018

- [13] Raj, N., Chandra, S., Priyadarshani, B. and **Ranjan, R.K.**, 2018, March. Multiple output current-controlled current conveyor transconductance amplifier using BiCMOS for analog signal processing. In *4th International Conference on Recent Advances in Information Technology (RAIT)*. IEEE.
DOI: [10.1109/RAIT.2018.8388989](https://doi.org/10.1109/RAIT.2018.8388989).
- [14] A. K. V Jha, V. K. Verma, P. Prince, B. Priyadarshini and **R. K. Ranjan**, "PSO Based Design of Current CCII-PID Controller for the Speed Control of BLDC Motor," *2018 International Conference on Power, Energy, Control and Transmission Systems (ICPECTS)*, Chennai, India, 2018, pp. 245-248.
DOI: [10.1109/ICPECTS.2018.8521567](https://doi.org/10.1109/ICPECTS.2018.8521567).
- [15] Kumari, S., Prince, P., Verma, V.K., Appasani, B. and **Ranjan, R.K.**, 2018, February. GA based design of current conveyor PLD controller for the speed control of BLDC motor. In *4th International Conference on Computational Intelligence & Communication Technology (CICT)* (pp. 1-3). IEEE.
DOI: [10.1109/CIACT.2018.8480149](https://doi.org/10.1109/CIACT.2018.8480149).
- [16] Tewary, S., Verma, V.K., Appasani, B., Gupta, P. and **Ranjan, R.K.**, 2018, February. Design of CCII PID Controller for the Control of Glucose Blood Level Using GA. In *4th International Conference on Computational Intelligence & Communication Technology (CICT)* (pp. 1-4). IEEE.
DOI: [10.1109/CIACT.2018.8480402](https://doi.org/10.1109/CIACT.2018.8480402).

Year 2017

- [17] Verma, V.K., Appasani, B., Gupta, P. and **Ranjan, R.K.**, 2017, September. GA based design of CCII PID controller for an inverted pendulum system. In *IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI)* (pp. 2721-2723). IEEE.
DOI: [10.1109/ICPCSI.2017.8392212](https://doi.org/10.1109/ICPCSI.2017.8392212).

- [18] Gupta, P., Appasani, B., Verma, V.K. and **Ranjan, R.K.**, 2017, September. PSO based CCII PID controller for a continuous stirred tank reactor system. In *IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI)* (pp. 2786-2789). IEEE. DOI: [10.1109/ICPCSI.2017.8392227](https://doi.org/10.1109/ICPCSI.2017.8392227).

Year 2016

- [19] Rani, N., **Ranjan, R.K.**, Pal, R. and Paul, S.K., 2016, March. Programmable and electronically tunable voltage-mode universal biquadratic filter based on simple CMOS OTA. In *3rd International Conference on Devices, Circuits and Systems (ICDCS)* (pp. 58-62). IEEE. DOI: [10.1109/ICDCSyst.2016.7570623](https://doi.org/10.1109/ICDCSyst.2016.7570623).

Year 2014

- [20] **Ranjan, R.K.**, Kumar, Y.S.P., Sorya, S., Paul, S.K. and Ghosh, M., 2014, February. Efficient Active Filter for filtering of harmonics in biomedical signal. In *International Conference BEATS-2014*, UIET, Chandigarh, India.

Year 2013

- [21] Ghosh, M., Paul, S.K., **Ranjan, R.K.** and Ranjan, A., 2013. Third order universal filter using single operational transresistance amplifier. *Journal of Engineering*, 2013(1), p.317296. DOI: [10.1109/CODEC.2012.6509217](https://doi.org/10.1109/CODEC.2012.6509217).

Ph.D. Student Supervision

S. No.	Name & Adm. No.	Registration & Status	Proposed Thesis Title
1	Pushkar Srivastava (17DP000209)	2017, Awarded	An Investigation into Selected Class of Non-Linear Analog Signal Processing Circuits
2	Vijay Kumar Verma (17DP000215)	2016, Awarded	Realization Of Active Control Circuits Using Current Mode Building Blocks
3	Somenath Dutta (17DP000255)	2016, Awarded	Design of Analog Signal Processing Circuits Using Analog Building Blocks
4	Niranjan Raj (17DR000367)	2017, Awarded	Study And Implementation of Novel Mem-Elements Emulator Circuit and Applications
5	Sagar (17DR000477)	2017, Awarded	Design And Performance Analysis of Memristor Emulator Circuit And Its Applications
6	Pankaj Kumar Sharma (17DR000641)	2017, Awarded	Study And Design of Mem-Element Emulators and Their Applications
7	Sadaf Tasneem (18DR0119)	2018, Awarded	Design And Performance Analysis of Fractional-Order Filters Using Current Mode Building Blocks
8	Dr. Prashant Kumar (19DR0108)	2019, Awarded	Design Of Memristor Emulator Circuits and Its Applications
9	Jagveer Singh Verma (18DP0002)	2018, Awarded	Design and Realization of CMOS-Based Memristor Emulator Circuits and their Applications
10	Rahul Ranjan (23DR0123)	2023, Ongoing	Low Power Memristor Design and Its Application In Neuromorphic Computing

S. No.	Name & Adm. No.	Registration & Status	Proposed Thesis Title
11	Ravi Jaiswal (23DP0030)	2023, Ongoing	Mixed-Signal Neuromorphic Architectures Leveraging Memristive Devices for Energy-Efficient Cognitive Processing
12	Basit Shafat Makhdoomi (23DR0212)	2023, Ongoing	Design of memelement based ultra low power neuromorphic spiking architecture and it's application
13	Shweta Kumari (23DR0317)	2023, Ongoing	Mixed-Signal Neuromorphic Circuits with Memristive Synapses for Real-Time Pattern Recognition
14	Niraj Kumar (24DP0098)	2024, Ongoing	Design and Development of Energy Storage Device
15	Sourav Maji (24DR0186)	2024, Ongoing	Memristive Mixed-Signal Neuromorphic Circuits: Models, Design Techniques, and Applications
16	Nitin Singhal (24DR0239)	2024, Ongoing	Design and Development of SNN Architecture for Smart Glass
17	Vedant Upadhyay (25DR0039)	2025, Ongoing	Hybrid CMOS-Based Mixed-Signal Neuromorphic Architecture for Edge Intelligence
18	Anurag Tyagi (25DP0063)	2025, Ongoing	Memristor-Based low power Mixed-Signal Neuromorphic Circuits for On-Board (Space Based flight) Processing
19	Kalakola Arun (25DR0286)	2025, Ongoing	Memristor-based Multilayer Neural Networks (MNN) and its Application in Neuromorphic System
20	Amarkant (26DR0005)	2026, Ongoing	Ultra-Low Power Neuromorphic Spiking Architecture for Assistive Smart Glass
21	Satyam Pandey (26DR0045)	2026, Ongoing	Ultra-Low Power Neuromorphic Spiking Architecture for Assistive Smart Glass

Current Research Associates under Sponsored Projects

S. No.	Name	Project No.	Project Title
1	Soumitra Das	(MeitY/2023-2024/1012/ECE)	Ultra-Low Power Neuromorphic Spiking Architecture for Assistive Smart Glass
2	Shweta Kumari	(MeitY/2023-2024/1012/ECE)	Ultra-Low Power Neuromorphic Spiking Architecture for Assistive Smart Glass
3	Amarkant	(MeitY/2023-2024/1012/ECE)	Ultra-Low Power Neuromorphic Spiking Architecture for Assistive Smart Glass
4	Arun Kalakola	(CSIR(40)/2023-2024/1045/ECE)	Memristor based Multilayer Neural Networks (MNN) and its Application in Neuromorphic System

M.Tech Student Supervision

S. No.	Name & Regd. No.	Year of Submission/Status	Thesis Title
1	Chandan Chaubey (2011MT0007)	May 2013	Study and Design of Analog and comb Filter using Current Mode Building Blocks
2	Kripa Sindhu Sharma (2010MT0139)	May 2012	De-Noising and detection of ECG Signal using Daubechies Wavelet
3	Ankita Sinha (2012MT0008)	May 2015	Design of Analog Signal and Generating Circuits
4	Satish Chandra (2013MT0152)	May 2015	Analog Signal Processing Circuits
5	Ravi Jaiswal (2013MT0275)	May 2015	Analog signal processing and generating circuits
6	Kundan Kumar (14MT000270)	May 2016	Study and design of current controlled current conveyor transconductance amplifier (CC-CCTA) and its application
7	Nishtha Rani (14MT000299)	May 2016	Study and design of memristor and analog filter using current mode building blocks
8	Nidhee Bhuwal (15MT000316)	May 2017	Study and Design of Emulator Circuit of Memristor, Memcapacitor and its application using Current mode building block
9	Bharti Kumari (15MT000162)	May 2017	Design of memristor emulator circuits using current mode building block
10	Prakhar Shrivastava (16MT000851)	May 2018	GT power engine model calibration of 4 cylinder gasoline direct injection SI engine
11	Subrato Roushan (16MT000879)	May 2018	Design of full wave rectifier circuits and instrumentation amplifier using current mode building block
12	Abhishek Shrivastav (16MT01161)	May 2018	Design of instrumentation amplifier and temperature sensor using current mode circuits
13	Rajesh Kumar Jena (17MT001605)	May 2019	Designing of Incremental and decremental Memristor Emulator Using MOSFET
14	Ravi Prakash (15KT000075)	May 2019	10T SRAM Cell Design
15	Kushagra Pandey (17MT001814)	May 2019	Analysis of 8 transistor SRAM cell
16	Ankush Gupta (20MT0070)	May 2022	Memristor emulator using single DDCCTA
17	Shweta Sonwani (20MT0385)	May 2022	Design and Implementation of Memristor emulator using current mode building block and its application
18	Shivam Singh (21MT0392)	May 2023	Electronically controllable multifunction fractional order filter
19	Shivendra Devivedi (22MT0096)	May 2024	CMOS Circuit Implementation of LIF hidden neuron model of an SNN for the wake up module

S. No.	Name & Regd. No.	Month & Year of Submission / Status	Thesis Title
20	Bediga Sreeram (23MT0096)	May 2025	Design of low/ ultra low power analog VLSI memristor emulator and its application in neuromorphic learning application
21	Ankit Saroj (23MT0059)	May 2025	Design and implementation of resource efficient camera interfacing architecture for real time image processing
22	Apoorv Pandey (24MT0077)	May 2026	Low Power Memristor Emulator and its Application in Mixed Signal
23	Aditya Bhusan (24MT0023)	May 2026	Design and implementation of camera interfacing architecture for real time image processing
24	Anami Satsangi (24MT0051)	May 2026	Digital memristor and its various applications
25	Aditya Sinha (25MT0029)	Ongoing	Yet to decide
26	Nabarun Biswas (25MT0297)	Ongoing	Yet to decide
27	Sachin Kumar (25MT0443)	Ongoing	Yet to decide

Facilities Available



Cadence Virtuoso

Industry-standard EDA tool for schematic-driven simulation and LVS-clean IC layout design.
Libraries: TSMC 180 nm, UMC 65 nm, SCL 180 nm.



OrCAD

Tool for schematic capture, mixed-signal simulation, and PCB design for manufacturing.
Library: TSMC 180 nm.

Major Positions / Achievement



Team Selected among the Top 37 teams nationwide for the prestigious **1TOPS (One Tape-Out Per Student) Program**, an initiative led by the VLSI Society of India (VSI)



Best Paper Award received by [Basit Shafat](#) for the paper titled “Memristor Emulator Circuit Design using MOCCII” presented at the *2024 International Conference on Modeling, Simulation & Intelligent Computing (MoSICom)*, Dubai, United Arab Emirates, IEEE, 2024.



Inder Mohan Thapar Award–2023 (Cash prize: Rs. 32000) for Best Publication, awarded to [Niranjan Raj](#), IIT (ISM) Dhanbad.



Top 2% Scientist Award (Stanford University, 2024).



Top 2% Scientist Award (Stanford University, 2023).



Mentor, IEEE USA section HAC Projects.



Shastri Institutional Collaborative Research Grant (SICRG), 2020.



Associate Editor, *Journal of Circuits, Systems, and Computers*.



Editor Manager, *AEÜ - International Journal of Electronics and Communications*.



Invited for [Chip Handover Ceremony](#) by Hon’ble Minister **Shri Ashwini Vaishnaw** at [SEMICON India Conference](#) (Sept 2025), New Delhi.

Reviewer Service

-  Microelectronics Journal (Elsevier)
-  Microsystem Technologies
-  Analog Integrated Circuits and Signal Processing
-  AEÜ - International Journal of Electronics and Communications
-  Circuits, Systems, and Signal Processing
-  IET Circuits, Devices & Systems
-  Journal of Circuits, Systems and Computers
-  Iranian Journal of Science and Technology (Transactions of Electrical Engg.)
-  IEEE Transactions on VLSI Systems
-  IEEE Transactions on Circuits and Systems I: Regular Papers
-  IEEE Transactions on Circuits and Systems II: Express Briefs
-  IEEE Sensors Journal
-  IEEE Journal on Emerging and Selected Topics in Circuits and Systems

Professional Memberships

-  Senior Member, IEEE (ID: 94456889).

Keynote Speaker & Invited Talks

-  Faculty Development Program on Advances in Analog and Mixed Signal Design (AAMSD-2025), **NIT Patna & DTU** (Aug 2025).
-  FDP on VLSI Devices, Circuits & Semiconductor Materials, **IIT Roorkee & MNIT Allahabad** (July–Aug 2025).
-  Smart Innovation in Semiconductor Devices, Photonics and Intelligent Automation (SISDPIA-2026), **Invited Speaker** (9 March-13 March 2026).

Administrative Responsibilities for IIT(ISM) Dhanbad

-  IR Duty, JEE Advanced Examination.
-  Member, DFSC of Electrical Engineering (Jan 2019 – Jan 2020).
-  Faculty Advisor, B.Tech ECE (Aug 2019 – Present).
-  Member, Selection Interview Boards for JRF (2016–2019, multiple phases).
-  Member, Centre of Societal Mission (CSM) (May 2017 – May 2020).
-  Hostel Warden (2017 – 2020).
-  Paper Setter, ISM EE Entrance Exam (M.Tech. ECE Programme, 2016).
-  Tabulator, Semester Examination (2017–18).
-  FIC, Departmental Time-table (2016–17).

Short-Term Courses, Workshops, Conferences & Meetings Organized

- ✎ Organizing Committee Member, International Conference on Microwave and Photonics (ICMAP) – 2013, 2015.
- ✎ Subject Expert, B. Tech Board of Course Studies (BOCS), BIT Sindri (June 2019).
- ✎ External Examiner, Viva-voce (VLSI Lab & GP), B. Tech ECE, BIT Sindri (Dec 2018).
- ✎ Organizer, One-week GIAN Course (Virtual) on *Memristor and its Application in Neuromorphic Computations*, June 23–27, 2025.
- ✎ Organizer, One-week IEP Course on *Advanced Semiconductor Design Techniques Using Modern VLSI EDA Tools*, July 13–17, 2026.
- ✎ Co-Organizer, Two-Week Offline Refresher Course on “**DEVICE-CIRCUIT CO-DESIGN: FROM EMERGING MATERIALS TO INTELLIGENT SYSTEMS**”, organized by Malaviya Mission Teacher Training Centre, IIT (ISM) Dhanbad, Aug. 2026.

Conferences & Seminars Attended

- 📅 RAIT-2018, Dhanbad, India.
- 📅 CICT-2018, Ghaziabad, India.
- 📅 ICPCSI-2017, Chennai, India.
- 📅 ICDCS-2016, Coimbatore, India.
- 📅 BEATS-2014, Chandigarh, India.
- 📅 CODEC-2012, Kolkata, India.
- 📅 RAIT-2012, Dhanbad, India.
- 📅 National Seminar on Renewable Energy Technology, Itanagar (2010).
- 📅 SEMICON India Conference (Sept 2025), New Delhi..

Workshops / Tutorials / STC Attended

- ✂ Advances in Device, Communication and IT, NERIST (July 2007).
- ✂ Winter School on VLSI Design, BIT Mesra (Dec 2011).
- ✂ Wireless and Wi-Max Issues, SLIET (July 2010).
- ✂ Managerial and Communicative Skills in the Era of Globalization, SLIET (July 2009).
- ✂ ASPECT-2013: Application of Simulators in Photonics, E & C Technology, Univ. of Calcutta.
- ✂ Workshop on Internet of Things, BIT Sindri (Oct 2019).

External Examiner for Thesis/Dissertation

- 👤 Served as External Examiner for M.Tech./Ph.D. thesis/dissertation evaluation at:
 - Birla Institute of Technology and Science (BITS), Pilani – Goa Campus
 - Thapar Institute of Engineering & Technology, Patiala
 - Birla Institute of Technology and Science (BITS), Pilani
 - Birla Institute of Technology, Mesra
 - National Institute of Technology (NIT), Surat
 - National Institute of Technology (NIT), Rourkela

Media Coverage

- Featured in **The Times of India** for work on IIT(ISM) Dhanbad's integrated circuit **APEEC1**, recognized at **Semicon India 2025**. Available at: [TOI News Article](#).
- Featured in **The Pioneer** for development of a Smart Auto-Irrigation and Soil Monitoring System by IIT(ISM) in 2022. Available at: [The Pioneer News Article](#).
- Featured in **Lagatar24 (English)** – IIT Dhanbad's Indigenous Chip **APEEC-1** Showcased at **Semicon India 2025**. Available at: [Lagatar24 News Article](#).
- Featured in **ETV Bharat (Hindi)** – India-made semiconductor chip: IIT(ISM) Dhanbad's major contribution. Available at: [ETV Bharat News Article](#).
- Featured in **Jagran** – IIT(ISM) Dhanbad develops smart irrigation system to help farmers in auto-irrigation. Available at: [Jagran News Article](#).
- Featured in **Shiksha.com** – IIT(ISM) Dhanbad develops auto-irrigation and soil monitoring system for COVID-19 affected farmer families. Available at: [Shiksha News Article](#).
- Featured in **The New Indian Express** – IIT(ISM) Dhanbad develops mobile app-based auto-irrigation system for migrants hit by COVID-19. Available at: [New Indian Express Article](#).
- Featured in **Jharkhand Mirror** – Auto-irrigation system by IIT(ISM) Dhanbad receives grant from IEEE USA. Available at: [Jharkhand Mirror Article](#).
- Featured in **Drishti IAS** – Auto-irrigation and soil monitoring system developed by IIT(ISM) Dhanbad featured in Jharkhand Current Affairs. Available at: [Drishti IAS Article](#).