इलेक्ट्रॉनिकी एवं
सूचना प्रौद्योगिकी मंत्रालय
MINISTRY OF
ELECTRONICS AND
INFORMATION TECHNOLOGY

सत्यमेव जयते

ChipIN

Chips to Startup Programme

Instruction Enhancement Program (IEP)

On

Advanced Semiconductor Design Techniques Using Modern VLSI EDA Tools

Schedule: 13 July 2026 to 17 July 2026 (Physical Mode)

Organised by:

Department of Electronics Engineering,
Indian Institute of Technology (ISM), Dhanbad

Funded by:

Ministry of Electronics and Information Technology,
Government of India

Abstract :

This five-day workshop on "Advanced Semiconductor Design Techniques Using Modern VLSI EDA Tools" is designed to provide participants with hands-on exposure to professional IC design methodologies. The program focuses on using Cadence Virtuoso for analog circuit design and Verilog-based digital design workflows, reflecting the practices followed in the semiconductor industry

Deadline - 30 June, 2026

Registration Link/QR code https://forms.gle/UUpswoNxSYcPjXeFA

Venue: New Lecture Hall (Lab 03), IIT(ISM) Dhanbad

ABOUT IIT (ISM), DHANBAD

Indian Institute of Technology (ISM) Dhanbad is a premier institution with a rich legacy of academic excellence, innovation, and research. Established in 1926, the institute has evolved into one of India's leading technical institutions and was accorded the status of an Indian Institute of Technology in 2016.

The institute offers world-class education and research facilities across engineering, science, management, and humanities disciplines, fostering innovation and industry engagement in emerging technological domains.

Established: 1926 **IIT Status:** 2016

Location: Dhanbad, Jharkhand

ABOUT THE DEPARTMENT

The Department of Electronics Engineering at IIT (ISM) Dhanbad is committed to excellence in education, research, and innovation in electronics, communication, and allied disciplines. Established as an independent department in 1998, it offers B.Tech., M.Tech., and Ph.D. programmes supported by experienced faculty members, advanced laboratories, modern computing facilities, and active research projects in emerging areas of electronics and communication engineering.

The curriculum is regularly updated to align with evolving technological trends and industry requirements while promoting innovation, interdisciplinary research, and industry collaboration.

Programmes Offered

- B.Tech. in ECE
- M.Tech. in VLSI Design
- M.Tech. in RF & Microwave
- M.Tech. in CSP
- M.Tech. in Photonics
- Ph.D. Programme

1998
Independent Department

UG, PG Ph.D.
Academic Programmes

Advanced
Research Laboratories

From Head's Desk

The Department of Electronics Engineering at IIT (ISM) Dhanbad has emerged as a vibrant centre for education, research, and innovation in a short span of time. Supported by dedicated faculty members, talented students, accomplished alumni, and modern laboratory infrastructure, the department continues to strengthen its presence in emerging areas of electronics, semiconductor technologies, VLSI design, embedded systems, artificial intelligence, and communication engineering.

Dr. Ravi Kumar Gangwar
Head, Department of Electronics Engineering
IIT (ISM) Dhanbad

"Shaping the Technology Leaders and Innovators of Tomorrow"

PROGRAMME OBJECTIVES & OUTCOMES

Programme Objectives

The Instruction Enhancement Program (IEP) on **Advanced Semiconductor Design Techniques Using Modern VLSI EDA Tools** is designed to provide participants with a comprehensive understanding of contemporary semiconductor technologies, integrated circuit design methodologies, simulation and verification workflows, FPGA-based hardware development, and emerging computing architectures. The programme covers key aspects of the semiconductor design cycle, ranging from device-level concepts and digital design fundamentals to system-level implementation and validation. Through expert lectures, interactive discussions, hands-on laboratory sessions, and practical demonstrations, participants will gain exposure to industry-standard EDA tools and modern design practices. The programme aims to equip faculty members, researchers, and students with the knowledge and practical skills required for semiconductor research, effective teaching, innovation, and product development in the rapidly evolving VLSI and semiconductor ecosystem.

5 Days | **6 Themes** | **7 Experts** | **Hands-on Labs**

Learning Outcomes

- Understand modern semiconductor device and IC design workflows.
- Gain practical exposure to Cadence Virtuoso design environment.
- Perform analog circuit design, simulation and optimization, understand physical design, DRC/LVS and sign-off verification.
- Learn digital system design using HDL and Verilog, develop FPGA-based hardware prototypes and interfaces.
- Explore emerging AI hardware and Bayesian accelerator architectures.
- Understand semiconductor manufacturing challenges and opportunities.
- Discover applications of ASICs and FPGAs in space systems.

Why Should You Join?

- Learn directly from experts from academia and industry.
- Gain hands-on experience with professional VLSI EDA tools.
- Connecting semiconductor knowledge with modern design practices, fabrication processes, and emerging applications.
- Explore current trends in semiconductor research and development, and understand India's growing semiconductor ecosystem.
- Develop skills relevant to higher studies and industry careers.
- Interact with researchers, faculty members and professionals.
- Receive a certificate upon successful completion of the programme.

Technical Themes

- Analog Circuit Design and Simulation Using Cadence tools.
- CMOS Analog Circuit Design
- Physical Design and Sign-Off Verification
- Digital System Design Using HDL and Verilog
- FPGA Design and Hardware Prototyping
- Hybrid CMOS–NVM AI Accelerators
- Semiconductor Manufacturing Technologies
- Mixed-Signal ASICs for Scientific Applications
- FPGA-Based Systems for Space Electronics

Bridging Semiconductor Theory, Design and Hardware Realization

KEY RESOURCE PERSONS

Prof. Tapan Kumar Gandhi, PhD, FNAE, FNASc., FAIIA, SMIEEE

He is a Professor in the Department of Electrical Engineering and Head of the Centre for Biomedical Engineering at IIT Delhi. His research spans Artificial Intelligence, Computational Neuroscience, Brain Imaging, Machine Learning, and Cognitive Computing. He has authored over 300 publications in leading journals including Science, Nature, PNAS, and IEEE Transactions, and holds six patents with multiple technology transfers. A Fellow of both FNAE and FNASc, he is a recipient of several prestigious awards, including the Abdul Kalam Technology Innovation National Fellowship.

Prof. Subindu Kumar

He is a Professor in the Department of Electronics Engineering, IIT (ISM) Dhanbad. His research interests include VLSI design, semiconductor devices, analog and mixed-signal ICs, embedded systems, and hardware implementation of intelligent systems. He has published extensively in reputed international journals and conferences and has guided numerous research scholars in the areas of microelectronics and integrated circuit design. He is actively involved in sponsored research, academic administration, and industry–academia collaborations.

Prof. Shubham Sahay

He is an Associate Professor in the Department of Electrical Engineering at IIT Kanpur and leads the Neuro Computing and Hardware Security (NeuroCHaSe) Research Group. His research focuses on neuromorphic computing, in-memory computing, hardware security, emerging nanoelectronic devices, and energy-efficient AI hardware. He has received several prestigious recognitions, including the IEEE EDS Early Career Award and the INAE Young Engineer Award. His work spans next-generation computing architectures, intelligent hardware systems, and secure edge-AI technologies.

Sh. H. S. Jatana

He is a distinguished semiconductor technologist and former Group Head at the Semi-Conductor Laboratory (SCL), Chanigarh Department of Space, Government of India. With more than three decades of experience, he has made significant contributions to CMOS technology, VLSI design, semiconductor process development, MEMS, and mixed-signal ASICs. He has played a pivotal role in the development of indigenous semiconductor technologies and has actively contributed to strengthening India's semiconductor ecosystem through research, technology development, and industry–academia collaborations.

Sh. Puneet Kumar

He is Senior Director, R&D - Emulation Solutions at Synopsys, with over two decades of experience in semiconductor design, functional verification, hardware emulation, and ASIC development. He leads advanced emulation and prototyping initiatives for next-generation SoC verification and has played a key role in developing industry-leading verification solutions. His expertise spans digital design, SystemVerilog, UVM, emulation platforms, and semiconductor workforce development through academia–industry engagement.

Sh. Anurag Tyagi

He is a Scientist/Engineer "SG" at the Space Astronomy Group (SAG), URSC, ISRO, with nearly two decades of experience in space-qualified detector electronics for X-ray, UV, and infrared payloads. He has contributed to major missions including Chandrayaan-1, Chandrayaan-2, Aditya-L1, and XPoSat, leading the development of advanced detector electronics and instrumentation. Currently, he serves as Deputy Division Head of the Payload Data Processing Division at SAG and actively contributes to India's space astronomy and planetary science missions.

Prof. Rahul Bhattacharya

He is an Assistant Professor in the Department of Electronics Engineering, IIT (ISM) Dhanbad. His research focuses on semiconductor devices, microelectronics, nanoelectronics, and VLSI technologies. He has published extensively in leading journals and conferences and is actively involved in research, teaching, and mentoring in advanced semiconductor and integrated circuit technologies.

PROGRAMME COORDINATION

Prof. Rajeev Kumar Ranjan

Coordinator
Department of Electronics Engineering
IIT (ISM) Dhanbad

Research Areas: Neuromorphic Computing, VLSI Design, Embedded Systems, Semiconductor Instrumentation

Prof. Manodipan Sahoo

Co-Coordinator
Department of Electronics Engineering
IIT (ISM) Dhanbad

Research Areas: Analog & Mixed-Signal IC Design, Microelectronics, Semiconductor Devices, VLSI Systems

PROGRAMME SCHEDULE

The five-day Instruction Enhancement Program (IEP) is designed to provide participants with comprehensive exposure to modern semiconductor design methodologies, analog and digital IC design, physical verification, FPGA-based system development, and emerging hardware technologies through expert lectures and hands-on laboratory sessions. The tentative day-wise schedule is presented below.

Tentative Time Table and Contents Of Course

Time	Day 1	Day 2	Day 3	Day 4	Day 5
9:00 to 9:30 AM	**Inauguration & Welcome**	**Opening Remarks**	**Opening Remarks**	**Opening Remarks**	**Valedictory Session**
9:30 to 11:00 AM	**Session 1:** Beyond the Basics: How Fundamental Science Paves the Way for Cures and Next Gen AI	**Session 3:** Latest Trends in Semiconductor Design and Verification	**Session 5:** Digital System Design with HDL	**Session 7:** Semiconductor Manufacturing Challenges and opportunities in India	**Session 9:** Applications of mixed signal ASICs and FPGAs for Space-Based Scientific Experiments
11:00 to 11:15 AM	**Tea Break**				
11:15 to 12:45 PM	**Session 2:** How to perform reliable and legitimate TCAD simulations?	**Session 4:** Hybrid CMOS-NVM Bayesian Inference Accelerators	**Session 6:** Digital System Design with Verilog	**Session 8:** CMOS Analog Physical Design	**Session 10:** Applications of mixed signal ASICs and FPGAs for Space-Based Scientific Experiments
12:45 to 1:45 PM	**Lunch Break**				
1:45 to 3:15 PM	**Lab 1:** Cadence Setup, Library Creation, and Schematic Capture	**Lab 3:** Analog Circuit Design and ADE Simulation Flow	**Lab 5:** Layout Design Using Cadence Virtuoso XL	**Lab 7:** DRC/LVS Verification and Antenna Rule Checking	**Lab 9:** FPGA Design Entry and HDL Implementation
3:15 to 3:30 PM	**Tea Break**				
3:30 to 5:00 PM	**Lab 2:** Analog Schematic Design Using Cadence Virtuoso	**Lab 4:** AC, Transient, and Noise Analysis of Analog Circuits	**Lab 6:** Post-Layout Simulation and Parasitic Extraction Flow	**Lab 8:** Sign-Off Verification, Padding, and GDSII Export	**Lab 10:** FPGA Camera Interfacing and Hardware Prototyping

Note: The schedule is tentative and may be modified based on programme requirements and the availability of resource persons. Detailed session timings and laboratory schedules will be communicated to registered participants.

REGISTRATION & PARTICIPATION DETAILS

Eligibility & Participation

Eligible Participants

- CI/Co-CI from the 100 C2S participating institutes.
- Additional faculty/staff from the same institute may be accommodated subject to availability.

Important Notes

- Participants should bring their own laptop.
- No TA/DA will be provided.
- Hostel accommodation may be arranged after selection, subject to availability, on payment of applicable hostel charges.
- Tea, snacks and working lunch will be provided during the sessions.

Important Dates

Registration Opens:
01 June 2026

Last Date of Registration:
30 June 2026

Confirmation of Selected Participants:
02 July 2026

Programme Duration: 13–17 July 2026

Programme Coordinators

Dr. Rajeev Kumar Ranjan
Coordinator
Department of Electronics Engineering
IIT (ISM) Dhanbad

Research interests include VLSI design, embedded systems, FPGA-based computing, and intelligent electronic systems.

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Dr. Manodipan Sahoo
Co-Coordinator
Department of Electronics Engineering
IIT (ISM) Dhanbad

Research interests include signal processing, machine learning, communication systems, and smart sensing technologies.

manodipan@iitism.ac.in

Registration & Contact Information

Registration Link:
https://forms.gle/m7TY3HnqxPQvA5yQ8

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Website: https://www.iitism.ac.in/electronics-engineering
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Participants may contact the programme coordinators regarding registration, accommodation, certificates and other programme-related queries.

Organizing Team

Student Coordinators

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Technical Support	Registration	Media & Publicity	Hospitality
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